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RECORD OF ORAL HEARING
UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte AKIHIKO KOH, TSUTOMU SAMPEI,
NOBUSHISA WATANABE and AKIHIRO KIKUCHI

Appeal 2009-004407
Application 09/802,857
Technology Center 2100

Oral Hearing Held: May 6, 2010

Before JAMES D. THOMAS, JOSEPH F. RUGGIERO and
MAHSHID D. SAADAT, *Administrative Patent Judges*

ON BEHALF OF THE APPELLANT:

BRIAN K. DUTTON, ESQ.
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1 THE CLERK: Calendar No. 21, Appeal No. 2009-4407. Mr.
2 Dutton?

3 JUDGE THOMAS: Thank you.

4 THE CLERK: Mm-hmm.

5 MR. DUTTON: Yes. We have a guest with me here. It's Ms.
6 Jiyeon Choi. She is a patent agent with our law firm, and has come to
7 observe.

8 Also, there are some other housekeeping issues --

9 Okay. I don't know --

10 JUDGE THOMAS: Have you been to the Board before, sir?

11 MR. DUTTON: Yes, I have.

12 JUDGE THOMAS: Okay. So you understand the time limits
13 and --

14 MR. DUTTON: Yes, I do.

15 JUDGE THOMAS: Just want to tell you we have a pretty good
16 understanding of the issues on the record.

17 MR. DUTTON: Okay.

18 JUDGE THOMAS: And you can proceed on that basis.

19 MR. DUTTON: Thank you, thank you very much.

20 I guess before I begin with my opening remarks, I just wanted
21 to ask the Board if there were any specific questions that the Board may
22 have, in order to expedite the process?

23 If not, then I shall begin.

24 May it please the Court, my name is Brian Dutton. I am
25 Counsel for Sony Corporation, the Appellant before this Court today.

26 The following issues before this Court is whether the Examiner
27 the Examiner erred in rejecting the claims in the present application.

28 We believe that the examples shown within the specification for
29 the present application are indeed commensurate with the scope of the
30 claims.

1 I would like to first discuss the Sagane reference. That
2 reference, the Examiner appears to have applied that reference as the
3 primary reference in the rejection of the claims on appeal.

4 Within that reference, there are two particular figures, Figure 1
5 and Figure 3, which are functional diagrams for the circuitry that the
6 Examiner has relied upon initially.

7 First starting out with Figure 3 of that reference, because I think
8 that's the easiest figure to discuss presently, if you look at Figure 3 of the
9 Sagane reference, you will notice that there is comparator 8. And that
10 comparator 8 has a signal, some sort of line A that goes to switch 23.

11 But what you don't see in Figure 3 of Sagane is a signal or some
12 other sort of system that's coming back into the comparator in the form of an
13 interrupt.

14 And that is one of our features of our claimed inventions, where
15 there is an interrupt that is received by the CPU, and which the process then
16 further advances, once the CPU processes this interrupt.

17 Now referring to Figure 1 of Sagane, again, we see here that
18 that is a comparator 8, but there is also now an interrupt control circuit 7D.

19 And then we see some sort of a line that comes from interrupt
20 control 7D, back to the CPU-2. Now the Examiner has identified CPU of
21 Sagane as being the CPU supposedly that would meet our claims.

22 Now as it turns out, upon a reading of the Sagane reference,
23 there is very little discussion, if any, about what that line is and how it
24 functions with the CPU.

25 Instead, many of the arguments and discussions about this
26 reference and about this figure refer to the interrupt control circuit, and what
27 the functions of the interrupt control circuit are in handling these instances,
28 where there is some sort of a data match in Element No. 9 of that reference.

29 So it's our position that the Sagane reference fails to show that
30 the CPU processes -- the CPU-2 -- processes in interrupt, upon receipt of
31 some sort of a coincidence between addresses that may be latched in
32 Element No. 9 of that reference.

1 Going on to the Suzuki reference, which I believe is probably
2 the next reference that the Examiner has applied, the Examiner has applied
3 that particular reference for the purposes of incrementing and decrementing.

4 And so the first point of that is that we believe that any other
5 discussion for any other purposes would amount to some sort of a new
6 ground that the Examiner has not put forth in the claims.

7 But now, one of the things with this Suzuki reference, with this
8 incrementing and decrementing function, is that our claims, specifically in
9 Claim 27, starting out, has a counter-register that is adapted to the store of
10 value, and where the value represents the number of times the interrupt
11 request signal indicates coincidence between the address and the bug
12 address.

13 That's within our Claim 27, for example.

14 Now with this Suzuki reference, as we have briefed in our
15 Appeal Brief and our Reply Brief, Figure 2B of this reference you can see in
16 Figure 2B that there is a most significant bit, which has the number of
17 portions of corrected portions.

18 We believe that that MSB unto itself fails to show how many
19 times this circuitry of Suzuki actually detects the number of coincidences.

20 All that this MSB circuitry seems to suggest to us is the number
21 of times or the number of corrections that are pre-programmed or
22 downloaded to the system, which is something totally different.

23 Now of course, the Examiner tries to address that function by
24 saying incrementing and decrementing are one and the same. But again, we
25 do not agree with that position, specifically, the circuitry required to
26 increment and the circuitry required to decrement are not the same circuits.

27 So of course, with that in mind, I guess in order to increment
28 would require a circuit that's different than what is disclosed within the
29 Suzuki reference.

30 I guess moving on to Claim No. 40, we have in this particular
31 claim the feature of the counter-reference adopted to store value, the value
32 representing again the number of times.

1 And again, we've talked about that with the Suzuki reference;
2 and again, wherein the value of the counter is incremented by 1. Again, that
3 was previously discussed.

4 Moving on to Claim No. 45, this is the claim where there are
5 multiple priority levels. And with this particular feature, I think it was that -
6 - I believe it was the Koscal reference that the Examiner has applied.

7 And one of the things with this Koscal reference is that that
8 reference fails to show an interrupt. There is no interrupt within the circuit
9 that goes back to the microcontroller or 102.

10 No interrupt. And if you look at Figure 1, you will not see this
11 interrupt.

12 Instead, all that this reference does is just merely places
13 different data on a bus. And that's about it. So this reference is not
14 dependent upon the interruption of the microcontroller, but instead, having
15 different data being placed on a data bus for its operating instruction.

16 And I guess also being a dependent claim this Hosotaini
17 reference, that the Examiner has applied, it appears to operate similar to the
18 Koscal reference, where all that is happening is that a different instruction
19 code is being placed on a bus, on the data bus, as opposed to having the
20 CPU-1 of the Hosotaini reference being interrupted.

21 And I guess finally, going to Claim No. 52, there are multiple
22 interruptions here that are ended together as a single interrupt.

23 The Examiner has applied the Hosotaini reference for this
24 particular feature. However, as we can see, looking at this reference,
25 everything coming from the OR gate goes to switches. Switches. Switch
26 10. None of the outputs from the OR gate 14 goes directly to the CPU.
27 None of it.

28 So therefore, the Hosotaini reference does not have the circuitry
29 to perform the invention, as we have claimed.

30 And I guess with that, I ask if there are any specific questions?

31 JUDGE THOMAS: Any questions from the panel?

32 JUDGE SAADAT: No questions.

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1 MR. DUTTON: Okay.
2 With that, I think you very much for your time.
3 JUDGE THOMAS: Thank you.
4 Whereupon, at 10:11 a.m., the proceedings were concluded.
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